	Type	Hits	Search Text	DBs	Time Stamp
2	BRS	12	circuit same latency same loop and (hdl or vhdl)	USPAT; US-PGPUB	2003/05/08 14:10
3	BRS	7	circuit same latency same loop and (hdl or vhdl)	USPAT; DERWENT	2003/05/08 14:08
4	BRS	64	circuit same delay same loop and (hdl or vhdl)	USPAT; DERWENT	2003/05/08 14:10
5	BRS	10	circuit same delay same loop and (hdl or vhdl) and pipeline	USPAT; DERWENT	2003/05/08 14:11

	Type	Hits	Search Text	DBs	Time Stamp
6	BRS	5	lock same step same consistency same check	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
7	BRS	593	lock same step same controller and code	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
8	BRS	41	lock same step same controller and code and emulator	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
9	BRS	66	lock same step same consistency	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
10	BRS	24	lock same step same consistency and controller and code	USPAT; US-PGPUB; DERWENT	2003/05/12 14:17
25	BRS	425	latency same delay same pipeline	USPAT; US-PGPUB; DERWENT	2003/05/29 15:49
26	BRS	39	latency same delay same pipeline and initiation	USPAT; US-PGPUB; DERWENT	2003/05/30 09:08

	Comments	Error Definition	Errors
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7			0
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26			0

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1994 , Grenoble, France

A VHDL-based design methodology: the design experience of a high performance ASIC chip

Authors
Maurizio Valle
Daniele Caviglia
Marco Cornero
Giovanni Nateri
Luciano Briozzo

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IEEE Computer Society Press Los Alamitos, CA, USA

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Year of Publication: 1994 – SEPTEMBER
ISBN:0-89791-685-9

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1994 , Grenoble, France

Scheduling of behavioral VHDL by retiming techniques

Authors
N. Wehn
J. Biesenack
Peter Duzy
T. Langmaier
M. Münch
Michael Pilsl
S. Rumler

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Year of Publication: 1994
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Citation

Annual ACM IEEE Design Automation Conference >archive
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1991 , San Francisco, California, United States

Scheduling for functional pipelining and loop winding

Authors
Cheng-Tsung Hwang
Yu-Chin Hsu
Youn-Long Lin

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SIGDA : ACM Special Interest Group on Design Automation
IEEE-CS : Computer Society

Publisher
ACM Press New York, NY, USA

Pages: 764 - 769 Series-Proceeding-Article
Year of Publication: 1991
ISBN:0-89791-395-7

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1992 , Anaheim, California, United States

High-level synthesis from VHDL with exact timing constraints

Authors
A. Stoll
P. Duzy

Sponsors
EDAC : Electronic Design Automation Consortium
IEEE-CS : Computer Society
IEEE-CAS : Circuits & Systems
SIGDA : ACM Special Interest Group on Design Automation

Publisher
IEEE Computer Society Press Los Alamitos, CA, USA

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ISBN:0-89791-516-X

INDEX TERMS

Primary Classification:
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B.5 REGISTER-TRANSFER-LEVEL IMPLEMENTATION

Citation

Annual ACM IEEE Design Automation Conference >archive
Proceedings of the 28th conference on ACM/IEEE design automation conference >toc
1991 , San Francisco, California, United States

CHOP: A constraint-driven system-level partitioner

Authors
Kayhan Kükçakar
Alice C. Parker

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SIGDA : ACM Special Interest Group on Design Automation
IEEE-CS : Computer Society

Publisher
ACM Press New York, NY, USA

Pages: 514 - 519 Series-Proceeding-Article
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Computer Design: VLSI in Computers and Processors, 1993. ICCD '93. Proceedings., 1993 IEEE International Conference on , 3-6 Oct 1993
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TI: **VHDL for High-Level Synthesis of Digital Systems**
Source: Proceedings of conference as follows from Dialog 165, Eventline:
EVENT TITLE: **1st European Working Conference on VHDL Methods**
EVENT DATE(S): September 4-7, 1990
HOST SITE: Inst. Mediterraneen de Techn.
EVENT CITY: Marseille
EVENT COUNTRY: France
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